#10/Appeal Brief 11/22/02 Hayes

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NEW DOCKET NO: OSEM-DB3

IN RE APPLICATION OF: Braddock Examiner: KANG

SERIAL NO: 09/636,484 GROUP ART UNIT: 2811

FILED: 08/10/00

TITLE: INTEGRATED TRANSISTOR DEVICES

TO: ASSISTANT COMMISSIONER OF PATENTS

COMBINED 37 CFR 1.192 APPEAL BRIEF
AND TRAVERSAL OF RESTRICTION

Sir: Responsive to the final office action dated 7/15/2002, the applicant appeals and traverses the restriction.

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TRAVERSAL OF THE ELECTION REQUIREMENT

The applicant traverses the restriction requirement on four grounds.

First, the examiner has not shown why claims 53-55 should be classified differently than claims 1-52. Claims 53-55 are method claims, but they are analogs of the structure claims in which similar elements are recited.

Second, the examiner has not shown that examining these claims would incur any additional burden.

Third, the similarity of the claimed subject matter strongly suggests that there would be no substantial burden in examining claims 53-55. Independent method claims 55 is identical to examiner structure claim 39, except for recitation of a "providing" or "depositing" of the elements recited in claim 39.

Fourth, the examiner's assertion that the structure claim could be made by a different process is incorrect because the allegedly different process is covered by claim 55. The examiner asserts that the "group II invention could be made by "a reverse order such as that [sic] forming a gate electrode on temporary substrate, forming a second layer on the gate electrode, forming a semiconductor wafer on the second layer, and then removing the temporary substrate" does not appear to provide a process distinct from the subject matter defined by claim 53.

For all of the foregoing reasons, the restriction requirement is improper and should be withdrawn. If it is not withdrawn, the examiner is obliged to make the restriction requirement final in the next communication so that the applicant can petition for removal of the restriction requirement and have that issued decided prior to a decision on the appeal.

37 CFR 1.192 APPEAL BRIEF

I. **37 CFR 1.192(a)**

This brief is being filed within 2 months from filing a notice of appeal. The notice of appeal and fee for the notice of appeal are filed herewith. [1] The brief is accompanied by the 37 CFR 1.17 fee and is filed in triplicate. The brief sets forth the authorities and argument the applicant will rely upon in the appeal.

II. **37 CFR 1.192(b)**

The appeal is timely and should not be dismissed.

III. **37 CFR 1.192(c)**

A. **Real Party in Interest**

The real party in interest is Osemi, Inc., which is wholly owned by David Braddock, the named inventor.

B. **Related Appeals and Interferences**

There are no related appeals or interferences.

C. **Status of Claims**

Claims 1-26 and 36-55 are pending. Claims 53-55 stand withdrawn. Claims 1-26, 37, and 39-52 stand allowed. Claims 36 and 38 stand rejected.[2]

D. **Status of amendments**

All amendments have been entered.

E. **Summary of the Rejected Inventions Under Appeal with Reference to Page and Line Numbers and Drawings**

The rejected inventions provide (claim 36) an enhancement mode metal-oxide-compound

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[1]Notice of appeal is submitted herewith.

[2]If the examiner withdraws the restriction requirement prior to decision on appeal, then claims 53-55 will be pending and not withdrawn, and either allowed or rejected. It those claims are rejected, the applicant will file a supplemental appeal brief directed to issues raised by their rejection.

semiconductor field effect transistor (Fig. 1 element 10) comprising:

a compound semiconductor wafer structure (Fig. 1 element 13 and page 6 line 8) having an upper surface;

a gate insulator structure (Fig. 1 element 30 and page 6 line 13) positioned on upper surface of said compound semiconductor wafer structure;

a gate electrode (Fig. 1 element 17 and page 6 line 20) positioned on upper surface of said gate insulator structure layer;

source and drain ion implants self-aligned to the gate electrode (Fig. 1 elements 21, 22; specification page 6 fourth line from bottom) ; and

source and drain ohmic contacts (Fig. 1 elements 19, 20 and page 6 fifth line from bottom) positioned on ion implanted source and drain areas;

wherein said compound semiconductor wafer structure comprises a Al_xGa_{1-x} As, In_yGa_{1-y}As, InP, or $In_zGa_{1-z}P$ layer (Fig. 1 element 15 and page 5 lines 19-20), said layer being positioned on said upper surface;

a substrate (Fig. 1 element 11 and page 6 line 12) on which resides said compound semiconductor wafer structure; and

wherein said substrate includes a InP based semiconductor wafer (page 5 third line from bottom).

The claim 38 invention also provides that "said transistor is integrated together with similar and complementary transistor devices to form complementary metal-oxide compound semiconductor integrated circuit." See the discussion of support in response to the 35 USC 112 rejection herein below with respect to this limitation.

F. **Issues**

I. Whether the rejection of claim 38 for lack of written description should be reversed.

II. Whether the rejections of claims 36 and 38 as obvious in view of US patent 5,945,718 to Passlack should be reversed.

G. **Groupings of Claims**

The claims do not stand or fall together.
Group 1 - Claim 36
Group 2 - Claim 38

H. **Argument (Reasoning)**

1. **Why Claims 36 and 38 Comply with 35 USC 103**

In rejecting claims 36 and 38 as obvious in view of the Passlack patent, the examiner states that:

Regarding claim 36, Passlack teaches an enhancement mode metal-oxide-compound semiconductor field effect transistor comprising (Fig. 1):

a compound semiconductor wafer structure (12) having an upper surface; a gate insulator structure (14) positioned on upper surface of said compound semiconductor wafer structure; a gate electrode (17) positioned on upper surface of said gate insulator structure layer; source (21) and drain (22) ion implants [sic] self-aligned to the gate electrode; and source and drain ohmic contacts (19 & 20) positioned on ion implanted source and drain areas, wherein said compound semiconductor wafer structure comprises a AlGaAs (23) and InGaAs (24) layers positioned on said upper surfaces; and a substrate (11) on which resides said compound semiconductor wafer structure. see also Col. 2,line 65 - Col. 4, line 4.

Passlack teaches the substrate includes comprises [sic] a GaAs but not InP. However, it is well known in the art and conventional to use the InP material asa substrate material (page 2, liens 16-18 in specification). Thus it would have been obvious in the art at the time the invention was made to substitute the GaAs of Passlack with well known InP since GaAs and InP both exhibit faster and more optimized speed/power performance.

Regarding claim 38, Passlack teaches an enhancement mode metal-oxide-compound compound semiconductor field effect tranasistor comprising (Fig. 1):

a compound semiconductor wafer structure (12) having an upper surface; a gate insulator structure (14) positioned on said upper surface; a gate electrode (17) positioned on upper surface of said gate insulator structure layer; source (21) and drain (22) ion implants [sic] self aligned to the gate electrode; and source and drain ohmic contacts (19 & 20) positioned on ion implanted source and drain areas, wherein the compound semiconductor wafer structure comprises a wider band gap spacer layer (23) and a narrower band gap channel layer (InGaAs, 24). See also Col. 2, line 65 - Col. 4 line 4.

Passlack does not show in Fig. 1 the transistor is integrated together with similar and complementary device to form complementary metal-oxide compound semiconductor integrated circuit. However, it is noted in the art that complementary GaAs exhibits optimum speed/power performance and efficiency at a low supply voltage of 1 V and below (see Col. 1, lines 22-24). Thus, it would have been obvious in the art at 6the time the invention was made to form CMOS device in order to provide high speed/power with lower power supply [Office action page 4 line 14 to page 6 line 2.]

In reply, the applicant disagrees with the examiner's statements of fact and conclusions of law.

a. **Additional Facts**

The applicant first points out the following additional facts and conclusions supported by the attached declaration of the inventor, David Braddock:

1. There is no AlGaAs composition for which lattice matching exists with InP.

Therefore, AlGaAs can not be grown epitaxially on InP with low defect densities. These facts are well known in the art.

2. Even for a composition containing as low as one percent GaP, $In_xGa_{1-x}P$ does not lattice match to an InP substrate. Therefore, InGaP cannot be grown epitaxially on InP with low defect densities. These facts are well known in the art.

3. The Passlack patent teaches using only AlGaAs or InGaP lattice matched to GaAs. The Passlack patent does not mention InP substrates. Passlack did not mention in the Passlack patent InP substrates presumably at least because he knew that his AlGaAs and InGaP devices grown on an InP substrate would not produce a useful device.

4. It is now known that stoichiometric Ga2O3 is an *n type semiconductor*, not an insulator. It has room temperature residual n type conductivity on the order of 10^{16} per cubic centimeter. That conductivity is much larger than the conductivity of insulating materials used as gate insulators. Materials used as gate insulators generally have conductivities of *less than* 10^{12} per cubic centimeter.

5. At the time Passlack filed for his patent, Dr. Braddock believes that Passlack did not know that stoichiometric Ga2O3 had a relatively large residual conductivity. Dr. Braddock speculates that Passlack filed for the Passlack patent assuming that residual conductivity of Ga2O3 was caused by defects, vacancies, or impurities and therefore Passlack thought that conductivity could potentially be reduced to a level at which his Ga2O3 would be commercially useful as a gate insulator.

6. The devices disclosed in the Passlack patent are not commercially useful. Ga2O3 does have a relatively large conductivity, which is one reason why the devices disclosed in the Passlack patent are not commercially useful.

7. The Passlack patent does not disclose a gate insulator. Instead, the Passlack patent discloses:

> The FET includes a *stoichiometric Ga2O3 gate oxide layer* positioned on upper surface of a compound semiconductor wafer structure. [Col. 2 lines 45-47; emphasis supplied.]

b. **Reasoning**

There is no motivation in the art to substitute InP for the substrate used by Passlack, for two reasons. First, there is no specific teaching of suggestion of such a modification of Passlack's teachings. Second, it is well known that such a substitution would prevent epitaxial low defect growth of either one of the AlGaAs and InGaP epitaxially grown materials disclosed in the Passlack patent.

Second, Passlack's stoichiometric Ga2O3 does not respond to the limitation defined in claims 36 and 38 of "a gate insulator structure." The first paragraph of the section of the specification of this application describing the invention defined the "gate insulator structure" recited in claims 36 and 38 as both electrically insulating and comprising at least two layers. That paragraph states in part:

> The present invention provides, among other things, a self-aligned

enhancement mode metal-oxide-compound semiconductor FET. The FET includes *a gallium oxygen insulating structure that is composed of at least two distinct layers.* The *first layer is* most preferably more that 10 angstroms thick but less that 25 angstroms in thickness and *composed substantially of gallium oxygen compounds including but not limited to stoichiometric Ga_2O_3 and Ga_2O, and possibly a lesser fraction of other gallium oxygen compounds.* The *upper insulating layer in the gallium oxide insulating structure* is composed of an insulator that does not intermix with the underlying gallium oxygen insulating structure. This upper layer must possess excellent insulating qualities, and is most typically composed of gallium oxygen and a third rare earth element that together form a ternary insulating material. *Therefore the entire gallium oxide rare earth gate insulator structure is composed of at least two layers* and may contain a third intermediate graded layers that consists of a mixture of the upper insulating material and the gallium oxygen compounds that compose the initial layer.

Please note that the specification was written by the inventor without advise of counsel, which explains in part the reference to two layers as "first layer" and "upper insulating layer" to the extent that that lack of clarity and any other descriptions that lack complete clarity cause the panel any confusion.

The specification contains specific references to "gate insulator structure" or the equivalent "gate insulating structure" all of which are consistent with a multi layer structure that is insulating to the extent necessary to form a useful gate insulator. See the recitations:

> A refractory metal gate electrode is preferably positioned on the upper surface of the gate insulator structure layer. [Page 5 lines 10-12.]
>
> Together the lower gallium oxide compound layer and the second insulating layer form a gallium oxide gate insulating structure. [Abstract.]
>
> The gallium oxide gate insulating structure and underlying compound semiconductor gallium arsenide layer (15) meet at an atomically abrupt interface at the surface of with the compound semiconductor wafer structure (14). [Abstract.]

Third, the Passlack patent does not disclose a gate insulator. The teachings of the Passlack patent do not enable one skilled in the art to form a structure containing a commercially useful device because the conductivity of the *stoichiometric Ga2O3 gate oxide layer* taught by Passlack is too high to be useful, the Passlack patent does not teach one or ordinary skill in the art this fact, and the Passlack patent does not teach one of ordinary skill in the art how to make a gate insulating structure having low enough conductivity to be useful.

2. **Argument (Reasoning) Respecting How Claim 38 Complies with 35 USC 112**

In rejecting claim 38 for lack of support, the examiner states that:

> The specification does not support the limitation "said transistor is integrated together with similar and complementary transistor devices to form complementary metal-oxide-compound semiconductor integrated circuit." [Office action page 4 lines 3-5.]

In reply, the applicant points out that the recited limitation is disclosed in the following locations:

The last sentence of the abstract states that:

> Multiple devices are then positioned in proximity and the appropriate interconnection metal layers and insulators are utilized in concert with other passive circuit elements to form a integrated circuit structure.

The abstract is part of the specification as filed as a matter of law.

The substitute specification in the field of the invention section states (page 1 lines 3-9) "The present invention pertains to ... fabrication of said structures and the ultra large scale integration of said transistors." Ultra large scale integration implies to one skilled in the art the use of complementary circuit architectures.

In the discussion of the background section (page 1 lines 11-13) identifies a problem addressed by the invention, which is that "The gallium arsenide and indium phosphide integrated circuit industry has been limited without a technology that simultaneously allows the integration of complementary field effect transistor devices and transistors with low gate leakage currents." Thus, the applicant clearly identifies the invention with integration of complementary field effect transistor devices and transistors.

The applicant specifically identifies application of his invention to large scale architectures, stating that "What is also needed are new and improved self-aligned compound semiconductor MOSFETs for use in complementary circuits and architectures. What is also needed are new and improved self-aligned compound semiconductor MOSFETs for low power/high performance complementary circuits and architectures. What is also needed are new and improved self-aligned compound semiconductor MOSFETs which offer the design flexibility of complementary architectures. "

In the specification of the invention section, the applicant states that:

> Thus, new and improved compound semiconductor devices and methods of fabrication are disclosed. The new and improved self-aligned enhancement mode metal-oxide-compound semiconductor heterostructure field effect transistors enable stable and reliable device operation, provide optimum compound semiconductor device performance for low power/high performance

complementary circuits and architectures, keep interconnection delay in ULSI under control, and provide optimum efficiency and output power for RF and microwave applications as well as for digital integrated circuits that require very high integration densities. [Page 9 lines 19-26.]

Furthermore, original claim 37 recited "integrated together with similar and complementary transistor devices to form complementary metal-oxide compound semiconductor integrated circuits."

Finally, Fig. 2 element 112 states "Provide Interconnection Means for the Formation of an Integrated Circuit" thereby conveying the concept of using multiple instances of a structure defined by the claimed invention.

Therefore, the applicant clearly disclosed that his invention was directed for use in integrated circuits including similar instances of the claimed transistor structure and in circuits using complementary (which means p and n type) devices. Therefore, the rejection of claim 38 for lack of support should be reversed.

IV. Claim Groups

A Group 1 - Claim 36

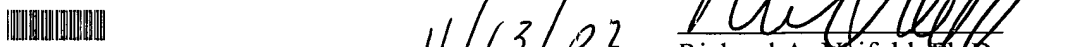
The obviousness rejection of claim 36 should be reversed because the Passlack patent does suggest either an "substrate includes a InP based semiconductor wafer"or a "gate insulator structure," as claimed.

B. Group 2 - Claim 38

The obviousness rejection of claim 38 should be reversed because the Passlack patent does suggest a "gate insulator structure," as claimed.

The 35 USC 112 rejection of claim 38 should be reversed because the specification discloses that the transistor structure embodiments are useful in integrated circuits including plurality of transistors and complementary structures.

Respectfully Submitted,



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APPENDIX - CLAIMS REJECTED AND UNDER APPEAL

Claims 36 and 38 read as follows:

36. (Amended) An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on upper surface of said compound semiconductor wafer structure;

a gate electrode positioned on upper surface of said gate insulator structure layer;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein said compound semiconductor wafer structure comprises a Al_xGa_{1-x} As, $In_yGa_{1-y}As$, InP, or $In_zGa_{1-z}P$ layer, said layer being positioned on said upper surface;

a substrate on which resides said compound semiconductor wafer structure; and

wherein said substrate includes a InP based semiconductor wafer.

38. A complementary metal-oxide compound semiconductor integrated circuit comprising an enhancement mode metal-oxide-compound semiconductor field effect transistor, said transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on said upper surface;

a gate electrode positioned on said upper surface;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas,

wherein the compound semiconductor wafer structure comprises a wider band gap spacer layer and a narrower band gap channel layer;

wherein the narrower band gap channel layer comprises $In_yGa_{1-y}As$; and

and wherein said transistor is integrated together with similar and complementary transistor devices to form complementary metal-oxide compound semiconductor integrated circuit.

APPENDIX 2 - ALL PENDING CLAIMS

The claims as amended appear below. All claims are reproduced for convenience.

1. (Amended) An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure comprising a first layer and a second layer;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising compounds of gallium and oxygen and at least one rare earth element;

a gate electrode positioned on said gate insulator structure;

source and drain ion implants self-aligned to said gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein gate electrode comprises a metal selected from the group consisting of W, WN, WSi , and combinations thereof.

2. (Amended) The transistor of claim 1 wherein said first layer forms an atomically abrupt interface with said upper surface.

3. (Amended) The transistor of claim 1 wherein said gate insulator structure is composed of at least three layers, including a graded layer that contains varying compositions of gallium oxygen and at least one rare-earth element.

4. (Amended) The transistor of claim 3 wherein said gate insulator structure further comprises at a third layer containing gallium and oxygen.

5. (Amended) The transistor of claim 1 said first layer has a thickness of more than 10 angstroms and less than 25 angstroms.

6. (Amended) The transistor of claim 1 wherein said gate insulator structure has a thickness of 20-300 angstroms.

7. (Amended) The transistor of claim 1 wherein said first layer forms an interface with said upper surface that extend less than four atomic layers in depth of structural interface modulation.

8. (Amended) The transistor of claim 1 wherein said first layer and said gate insulator structure protects said upper surface.

9. (Amended) The transistor of claim 1 wherein said gate electrode comprises a refractory metal which is stable in presence of the top layer of the gate insulator structure at 700°C.

10. (Amended) The transistor of claim 1 wherein said source and drain ion implants provide one of an n-channel or p-channel.

11. (Amended) The transistor of claim 1 wherein said source and drain ion implants comprise at least one of Be/F and C/F.

12. (Amended) The transistor of claim 1 wherein said upper surface comprises GaAs.

13. (Amended) The transistor of claim 1 wherein said upper surface comprises $In_xGa_{1-x}As$.

14. (Amended) An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

gate insulator structure on said upper surface, said gate insulator structure comprising a first layer, a second layer, and a third layer;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer substantially comprising compounds of gallium and oxygen and at least one rare earth element such that the normalized relative composition of at least one of gallium, oxygen, and said at least one rare earth element in said second layer varies in a monotonic manner as a function of depth within said second insulating layer;

said third layer above said second layer, said third layer substantially comprising gallium oxygen and at least one rare earth element, said third layer being insulating;

a gate electrode positioned on said gate insulator structure;

source and drain ion implants self-aligned to said gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein said gate electrode comprises a metal selected from the group consisting of W, WN, WSi , and combinations thereof.

15. (Amended) The transistor of claim 14 wherein said first layer forms an atomically abrupt interface with said upper surface.

16. (Amended) The transistor of claim 14 wherein the gate insulator structure comprises a varying layer that substantially comprises gallium, oxygen, and at least one rare-earth element in which relative concentration of at least one of gallium, oxygen, and said at least one rare earth in said varying layer monotonically vary with depth in said layer.

17. (Amended) The transistor of claim 14 wherein said first layer has a thickness of more than 10 angstroms and less than 25 angstroms.

18. (Amended) The transistor of claim 14 wherein the gate insulator structure has a thickness of 20-300 angstroms.

19. (Amended) The transistor of claim 14 wherein said first layer forms an interface with the compound semiconductor wafer structure that extend less than four atomic layers in depth of modulation of said interface.

20. (Amended) The transistor of claim 14 wherein said first layer and said gate insulator structure protects said upper surface.

21. (Amended) The transistor of claim 14 wherein said gate electrode comprises a metal which is stable in presence of the top layer of the gate insulator structure at 700°C.

22. (Amended) The transistor of claim 14 wherein said source and drain ion implants define an n-channel.

23. (Amended) The transistor of claim 14 wherein said source and drain ion implants comprise and Be/F and C/F, and define a p-channel.

24. (Amended) The transistor of claim 14 wherein said upper surface comprises GaAs.

25. (Amended) The transistor of claim 14 wherein said upper surface comprises $In_xGa_{1-x}As$.

26. An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a multilayer gate insulator structure positioned on said upper surface, said multilayer gate insulator structure substantially comprising alternating layers each of which comprises gallium, oxygen, and at least one rare-earth element;

a gate electrode positioned on said multilayer gate insulator structure;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

and dielectric spacers positioned on sidewalls of said gate electrode.

27-35. - Canceled by this amendment.

36. (Amended) An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on upper surface of said compound semiconductor wafer structure;

a gate electrode positioned on upper surface of said gate insulator structure layer;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein said compound semiconductor wafer structure comprises a Al_xGa_{1-x} As, $In_yGa_{1-y}As$, InP, or $In_zGa_{1-z}P$ layer, said layer being positioned on said upper surface;

a substrate on which resides said compound semiconductor wafer structure; and

wherein said substrate includes a InP based semiconductor wafer.

37. (Amended) A complementary metal-oxide compound semiconductor integrated circuit comprising the transistor of claim 1, 13, or 26 integrated together with similar and complementary transistor devices to form said complementary metal-oxide compound semiconductor integrated circuit.

38. A complementary metal-oxide compound semiconductor integrated circuit comprising an enhancement mode metal-oxide-compound semiconductor field effect transistor, said transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on said upper surface;

a gate electrode positioned on said upper surface;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas,

wherein the compound semiconductor wafer structure comprises a wider band gap spacer layer and a narrower band gap channel layer;

wherein the narrower band gap channel layer comprises $In_yGa_{1-y}As$; and

and wherein said transistor is integrated together with similar and complementary transistor devices to form complementary metal-oxide compound semiconductor integrated circuit.

39. An enhancement mode metal-oxide-compound semiconductor field effect transistor structure, comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure comprising a first layer and a second layer, said gate insulator on said upper surface;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising at least one compound of gallium, oxygen and at least one rare earth element; and

a gate electrode positioned on said gate insulator structure.

40. The structure of claim 39 wherein said gate electrode comprises a refractory metal.

41. The structure of claim 39 wherein said gate electrode comprises a member of the group consisting of W, WN, WSi , and combinations thereof.

42. The structure of claim 39 wherein said gate insulator structure further comprises a third layer.

43. The structure of claim 42 wherein said third layer comprises compounds comprising gallium and oxygen.

44. The structure of claim 43 wherein compounds of said third layer comprising gallium and oxygen further comprise a rare earth element.

45. The structure of claim 44 wherein a composition of said third layer varies monotonically with depth in said third layer.

46. The structure of claim 43 wherein said gate insulator structure further comprises a fourth layer.

47. The structure of claim 43 wherein said fourth layer comprises compounds comprising gallium and oxygen.

48. The structure of claim 47 wherein compounds of said fourth layer comprising gallium and oxygen further comprise a rare earth element.

49. The structure of claim 39 wherein said first layer is adjacent and in contact with said upper surface.

50. The structure of claim 39 further comprising source and drain contacts.

51. The structure of claim 39 wherein said source and drain contacts are rapid thermal annealed in UHV.

52. The structure of claim 39 wherein said gate insulator structure passivates said upper surface.

53. A method for forming an enhancement mode metal-oxide-compound semiconductor field effect transistor structure, comprising:

providing a compound semiconductor wafer structure having an upper surface;

depositing a gate insulator structure comprising depositing a first layer and depositing a second layer, said gate insulator on said upper surface;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising at least one compound of gallium, oxygen and at least one rare earth element; and

depositing a gate electrode positioned on said gate insulator structure.

54. The method of claim 53 comprising rapid thermal annealing said structure in UHV.

55. The method of claim 54 wherein said rapid thermal annealing comprising annealing at between 700 and 900 degrees Centigrade.

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